ABSTRACT OF THE DISCLOSURE

A content addressable memory (CAM) device having circuitry to generate a biased sequence of addresses. A first counter circuit increments an address value in response to a clock signal and resets the address value to a start address in response to a control signal. A second counter increments a limit value in response to a control signal. A compare circuit compares the address value and the limit value and, if the address value and the limit value have a predetermined relationship, asserts the control signal.